REMARKS

This is a full and timely response to the outstanding non-final Office action delivered on August 11, 2009. Reconsideration of the present application in light of the following grounds is respectfully requested.

Present Status of the Application

In the Office action, claims 15 and 16 are rejected under 35 U.S.C 102(b) as being anticipated by Jun (U.S. Publication No. 2003/0117350; "Jun" hereinafter). Claims 1-4, 6-8, 12, 17-26 and 30 are rejected under 35 U.S.C. Section 103(a) as being unpantentable over Akahori (U.S. Publication No. 2005/0012705; "Akahori" hereinafter). Moreover, claims 9-11 and 27-29 are rejected under 35 U.S.C 103(a) as being patentable over Akahori in view of Jun.

In response thereto, Applicant has amended claims 1, 6-9, 11, 15-16, 18-19, 24-27 and 29-30, and the written support of the amendments is provided in Fig.5, Fig. 6 and paragraph [0026] and [0027] of present application. Therefore, it is submitted no new matter is introduced by the proposed amendments. Furthermore, Applicant has canceled claims 10, 12, 17 and 28. Currently, claims 1-4, 6-9, 11, 15-16, 18-27 and 30 remain pending in the application.

Discussion of Office Rejections under 35 U.S.C. Section 102

Claims 15 and 16 are rejected under 35 U.S.C 102(b) as being anticipated by Jun.

Applicant respectfully disagrees.

In order to clearly distinguish the present invention from the Jun reference, the amended claim 15 is recited below.

"15. A gate driver, suitable for use in a panel display apparatus to drive corresponding pixels, comprising:

a gate input interface, receiving a serial-protocol image display signal and a clock pair signal, wherein the serial-protocol image display signal and the clock pair signal are continuously transmitted to a next one of the gate driver **and the image display signal includes a red pair signal, a green pair signal and a blue pair signal, the red pair signal, the green pair signal, the blue pair signal and the clock pair signal are used for decoding out a plurality of control signals for gate drivers**; and

a state-in-the-art gate driver, respectively receiving the control signals for gate drivers gate input signals,

wherein the serial-protocol image display signal is at least one of red or green or blue pair signals." (Emphasis added)

The Office action holds that Jun teaches claim 15 of present application by Fig.1 and paragraph [0011]-[0013]. Applicant indicates that Jun discloses that "[t]o achieve the above and other objects, the present invention may be accomplished by providing a liquid crystal display (LCD) apparatus equipped with an image processor and a liquid crystal panel having a matrix array formed with liquid crystal pixels to display video data processed by the image processor on a screen, including: liquid crystal pixel drivers connected in series; driver arrays driving the liquid crystal pixel drivers; and **a timing controller converting the video data into serial data bit streams and transmitting the serial data bit streams to the driver arrays**, so that the driver arrays control each liquid

crystal pixel driver to receive the serial data bit streams respectively" in paragraph [0011]. That is, Jun discloses **a timing controller for converting the video data into serial data bit streams** in paragraph [0011].

Moreover, Jun discloses "[t]he liquid crystal pixel driver includes a by-pass set-up register and each of the serial data bit streams includes a by-pass set-up bit stream to set up the by-pass set-up register to allow respective data to be stored in the corresponding liquid crystal pixel driver. The liquid crystal pixel driver includes a clock signal line, a word signal line distinguishing a word unit, a command code and a command data unit of the serial data bit stream, a data signal line, and a command/data selection signal line to select a command data or the video data for the respective serial data bit stream inputted into the data signal line. **The timing controller selects the command/data selection line of each of the liquid crystal pixel drivers to allow the command to be inputted, and determines a data bit stream from the data signal line according to a signal level of "high" or "low" of the word signal line as the command code or the command data**" in paragraph [0012]. Applicants indicate that Jun discloses **a timing controller selects the command/data selection line of each of the liquid crystal pixel drivers to allow the command to be inputted, and determines a data bit stream from the data signal line according to a signal level of "high" or "low" of the word signal line as the command code or the command data**. That is, there is a command decoder for the LCD driver needed to decode the command/data selection line selected by the timing controller.

Please notice here, Applicant submits that the amended claim 15 of present

application discloses that "**the image display signal includes a red pair signal, a green pair signal and a blue pair signal, the red pair signal, the green pair signal, the blue pair signal and the clock pair signal are used for decoding out a plurality of control signals for gate drivers**". That is, the amended claim 15 of present application discloses to decode out the clock pair signal and the red, blue and green pair signals into a plurality of control signals for gate driver. Apparently, there is no command/data selection line needed in the amended claim 15 and a person skilled in the art knows that the command/data selection line is used for a timing controller to inform the LCD driver the incoming data stream is command code or data code.

Besides, Jun also discloses "[t]he timing controller selects the command/data selection line of each of the liquid crystal pixel drivers to allow the data to be inputted, and determines a data bit stream from the data signal line according to a signal level of "high" or "low" of the word signal line as an RGB video data. In a case where a by-pass bit is established in the by-pass set-up register of each of the liquid crystal pixel drivers, the data bit stream is transmitted into an adjacent liquid crystal pixel driver. Further, each of the liquid crystal pixel drivers is a gate driver to select a column line of the matrix array" in paragraph [0013]. Although Jun has disclosed RGB video data, Jun fails to disclose to decode the RGB video data into the control signal for the gate drivers. Accordingly, Jun fails to disclose the amended claim 15 and the rejection should be withdrawn.

Further, regarding claim 16 of present application, the Office also holds that Jun teaches claim 16 in Fig. 1 and paragraph [0011-0013]. Applicant indicates that Jun fails to teach control signals for the source drivers include a clock signal and an identification

information, and the clock signal and the identification information is in accordance with the switch unit to pass the serial-protocol image display signal and the clock pair signal to the next one of the gate driver or export the clock signal to the state-in-the-art gate driver.

Accordingly, Jun also fails to disclose the amended claim 16 and the rejection should be withdrawn.

Discussion of Office Rejections under 35 U.S.C. Section 103

Claims 1-4, 6-8, 12, 17-26 and 30 are rejected under 35 U.S.C. Section 103(a) as being unpantentable over Akahori. Claims 9-11 and 27-29 are rejected under 35 U.S.C 103(a) as being patentable over Akahori in view of Jun. Applicant respectfully disagrees.

In order to clearly distinguish the present invention from the Akahori reference, the amended claim 1 is recited below.

"1. A serial-protocol panel display system, suitable for use in a panel display apparatus, comprising:

a pixel-array unit;

a video graphic adapter (VGA) unit, according to a serial protocol, to export a serial-protocol image display signal and a clock pair signal, wherein the image display signal includes a red pair signal , a green pair signal and a blue pair signal; and

a plurality of gate drivers and source drivers, coupled to the video graphic adaptor unit and the pixel-array unit, the gate and the source drivers receiving the clock pair signal, the red pair signal, the green pair signal and the blue pair signal, the gate and the source drivers decode the clock pair

signal and at least one of the red or the green or the blue pair signals to obtain a plurality of input signals for driving the pixel-array unit to display image."
(Emphasis added)

The Office action holds that Akahori discloses claim 1 of present application in Fig. 1 and Fig. 2. In response thereto, Applicant has amended claim 1 and indicates that Akahori fails to disclose "**the source drivers decode the clock pair signal and at least one of the red or the green or the blue pair signals to obtain a plurality of input signals for driving the pixel-array unit to display image".** Firstly, the Office recites that Akahori fails to teach the serial protocol image display signal is at least one of red or green or blue pair signal. (Office Action: page 4, third paragraph). Apparently, Akahori fails to disclose to decode the **at least one of the red or the green or the blue pair signals to obtain a plurality of input signals.**

Secondly, in the Akahori's disclosure about Fig. 1 and Fig.2, Akahori discloses "[a] system comprising a display device of the present invention is made up of a display panel 100 such as a liquid crystal or plasma display, **a source driver 101 which supplies pixel data to the display panel 100, a gate driver 102 which drives the gates of pixels to be scanned by one horizontal scan line on the display panel 100 and supplies the data from the source driver 101 to the pixels, and a controller 103 which supplies a start pulse S, data D, and a clock C to the source driver 101 and supplies a scan horizontal sync signal and the like to the gate driver 102**" in paragraph [0029], and "[t]he source driver 101 consists of cascade-connected driver ICs 1011 to 101n. **A driver**

IC 1011 receives a start pulse S, data D, and a clock C from the controller 103, transmits these signals to a driver IC 1012, and the driver IC 1012 and subseqent driver ICs receive these signals from the preceding-stage driver and supply the signals to the following-stage driver IC and eventually the driver IC 101n receives these signals" in paragraph [0030].

Moreover, Akahori also discloses "[t]he driver IC 2011, as is shown in FIG. 2, comprises **a start pulse input terminal for receiving a start pulse from the controller 103, a data input terminal for receiving data, a clock input terminal for receiving a clock, an internal circuit 2021, a switch 2031, a start pulse output terminal for outputting the start pulse to the next-stage driver 2012, a data output terminal for outputting the data, and an output terminal for outputting the clock**." In paragraph [0031] and "[t]he start pulse is transmitted from the start pulse input terminal to the start pulse output terminal, the data is transmitted from the data input terminal to the data output terminal, and the clock is transmitted from the clock input terminal to the clock output terminal through internal wiring of the driver IC and the switch 2031. Note that all these signals are not routed through the internal circuit 2021 to the output terminals. Thus, the start pulse and the data/clock do not fall out of sync, which could take place in a similar prior-art device because the start pulse is supplied on a different path from the transmission paths of the data/clock in the prior-art device. The reliability in data capturing is enhanced and the driver ICs robust to high clock frequencies can be realized" in paragraph [0032].

That is, Akahori discloses a controller transports control signals such as start pulse,

data and clock signal, and driver receives to control signal to drive o corresponding pixels. There is no disclosure about the technical feature **control signals are obtained by decoding the clock pair signals and at least one of the red, green and blue pair signals**. That is, Akahori fails to disclose the amended claim 1 of present application.

Besides, Applicant has amended claims 6-9 and 11 according to the independent claim 1. Since claims 6-9 and 11 depend on the allowable claim 1, these dependent claims should also be non-obvious and allowable. The 103 rejections of claims 6-9 and 11 should also be withdrawn.

For the same reason discussed about claim 1, Applicant has amended claims 18 and 19 by adding the limitation of decoding the red pair signal, the green pair signals, the blue pair signal and the clock pair signal to obtain the control signals. That is, the rejection to the amended claims 18 and 19 should be withdrawn.

Since claims 2-4 and claims 20-23 respectively depend on the allowable claims 1 and 19, these dependent claims should also be non-obvious and allowable. The 103 rejections of claims 2-4 and 20-23 relying upon the reference should also be withdrawn.

Besides, Applicant has amended claims 24-27, 29 and 30 according to the independent claim 19. Since claims 24-27, 29 and 30 depend on the allowable claim 19, these dependent claims should also be non-obvious and allowable. The 103 rejections of claims 24-27, 29 and 30 should also be withdrawn.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-4, 6-9, 11, 15-16, 18-27 and 30 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Office believes that a telephone conference would expedite the examination of the above-identified patent application, the Office is invited to call the undersigned.

Respectfully submitted,

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James A. Long
Registration No.: 62,006

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: Usa@jcipgroup.com.tw